

CLAIMS

1. A tip attached to a chip component for making a readable change into a storage medium, the tip comprising:
 - a conductive layer;
 - a tip sub-layer made of amorphous silicon disposed on the conductive layer; and
 - an outer layer disposed on the tip sub-layer formed of a silicide material;wherein the chip component is constructed with at least one type of metal material;
- wherein the silicide includes a metal having a silicide formation temperature below a melting temperature of the metal material of the chip component.
2. The tip according to claim 1, wherein the chip component is an IC electrical component.
3. The memory storage device according to claim 1, further comprising a nitride layer disposed on the outer layer.
4. The tip according to claim 1, wherein the metal of the silicide is Platinum or Palladium.
5. The tip according to claim 1, wherein the metal of the silicide is iron, chrome, nickel, niobium, or molybdenum.
6. The tip according to claim 1, wherein the melting temperature is at or below 500 Degrees C.

7. A memory storage device comprising:
 - a chip component including a metal material;
 - a tip connected to the chip;
 - a storage medium in contact with the tip;
 - wherein the tip comprises:
 - a conductive layer;
 - a tip sub-layer made of amorphous silicon disposed on the conductive layer; and
 - an outer layer disposed on the tip sub-layer formed of a silicide;
 - wherein the silicide includes a metal having a silicide formation temperature below a melting temperature of the metal material of the chip component.
8. The memory storage device according to claim 7, wherein the chip component is an IC electrical component.
9. The memory storage device according to claim 7, further comprising a nitride layer disposed on the outer layer.
10. The memory storage device according to claim 7, wherein the metal of the outer layer is platinum or palladium.
11. The memory storage device according to claim 7, wherein the forming temperature is at or below 500 Degrees C.
12. The memory storage device according to claim 7, wherein the metal of the outer layer is iron, chrome, nickel, niobium, or molybdenum.

13. A method for forming a tip that creates a readable change in a media on a storage medium, the method comprising the steps of:

- providing a conductive substrate;
- disposing an amorphous silicon layer on the substrate;
- removing portions of the amorphous layer to form a tip sub-layer;
- disposing a metal layer on the tip sub-layer; and
- annealing the tip sub-layer and metal layer at or below a melting temperature of the metal material of the chip component.

14. The method according to claim 13, further comprising disposing a nitride layer on the silicide layer.

15. The method according to claim 14, wherein the nitride layer is disposed on the silicide layer during the step of annealing.

16. The method according to claim 13, wherein the removing step further comprises:

- disposing a mask layer on the amorphous silicon layer;
- etching the mask layer into a block pattern; and
- etching the amorphous silicon layer around the block pattern to form the tip sub-layer.

17. The method according to claim 13, further comprising electrically connecting the conductive layer to a chip component.

18. The method according to claim 13, wherein the metal layer is constructed of platinum or palladium.

19. The method according to claim 18, wherein the metal material of the chip component includes aluminum.

20. The method according to claim 19, wherein the chip component is an IC electrical component.

21. The method according to Claim 15, wherein the forming temperature is at or below 500 Degrees C.

22. A tip for forming a readable change in the media, the tip comprising:

conductive layer means for effectuating electrical conduction between a chip component and an external component;

a tip sub-layer means made of amorphous silicon disposed on the conductive layer; and

an outer layer means for forming a silicide with the tip sub-layer at an anneal temperature below a temperature that causes damage to the chip component.